MITSUBISHI ELECTRIC

Specifications are subject to change without notice.

< S-band High Power GaN HEMT >

MGFS38G38L2-01

2.5 – 3.8 GHz / 7W(Psat) x 2

DESCRIPTION

The MGFS38G38L2, GaN HEMT with an N-channel Schottky gate, is designed for S-band base transmitter station applications.

FEATURES

- High Voltage Operation : VDS=50V
- High Output Power : 38dBm (typ.) @ Psat, f=3.5GHz, Single Path
- High Efficiency : 60% (typ.) @ Psat, f=3.5GHz, Single Path
- High Gain : 18dB (typ.) @ f=3.5GHz, Single Path

APPLICATION

- Amplifier for S-band Base Transmitter Station

RECOMMENDED BIAS CONDITIONS

- Vds=50V • Ids=30mA

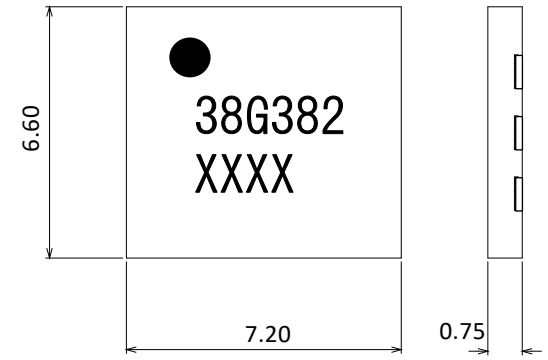
Absolute Maximum Ratings (Case Temperature Tc=25°C)

Symbol	Parameter	Ratings	Unit
VDS	Operating Voltage	55	V
VBR	Drain-Source Voltage (V_{GS}=-5V)	150	V
VGS	Gate–Source Voltage	-15	V
PT	Total Power Dissipation	13	W
Pin	Maximum Input Power	27	dBm
Tch	Channel Temperature	200	°C
Tstg	Storage Temperature	-55 to +150	°C

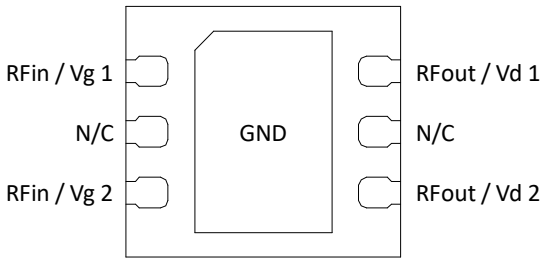
Recommended Operating Conditions

Symbol	Parameter	Limit	Unit
VDS	Operating Voltage	≦50	V
IGF	Forward Gate Current (RG=10Ω, Single Path)	≦6	mA
IGR	Reverse Gate Current (RG=10Ω, Single Path)	≦0.75	mA
Tch	Channel Temperature	≦185	°C
Pave	Average Output Power (Single Path)	30	dBm

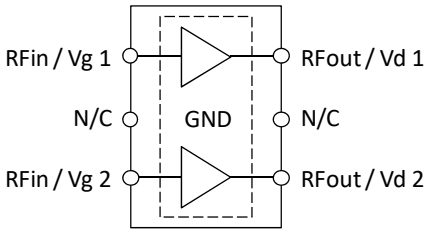
Outline Drawing [unit : mm]



[Perspective View]



[Block Diagram]



Electrical Characteristics (Case Temperature Tc=25°C)

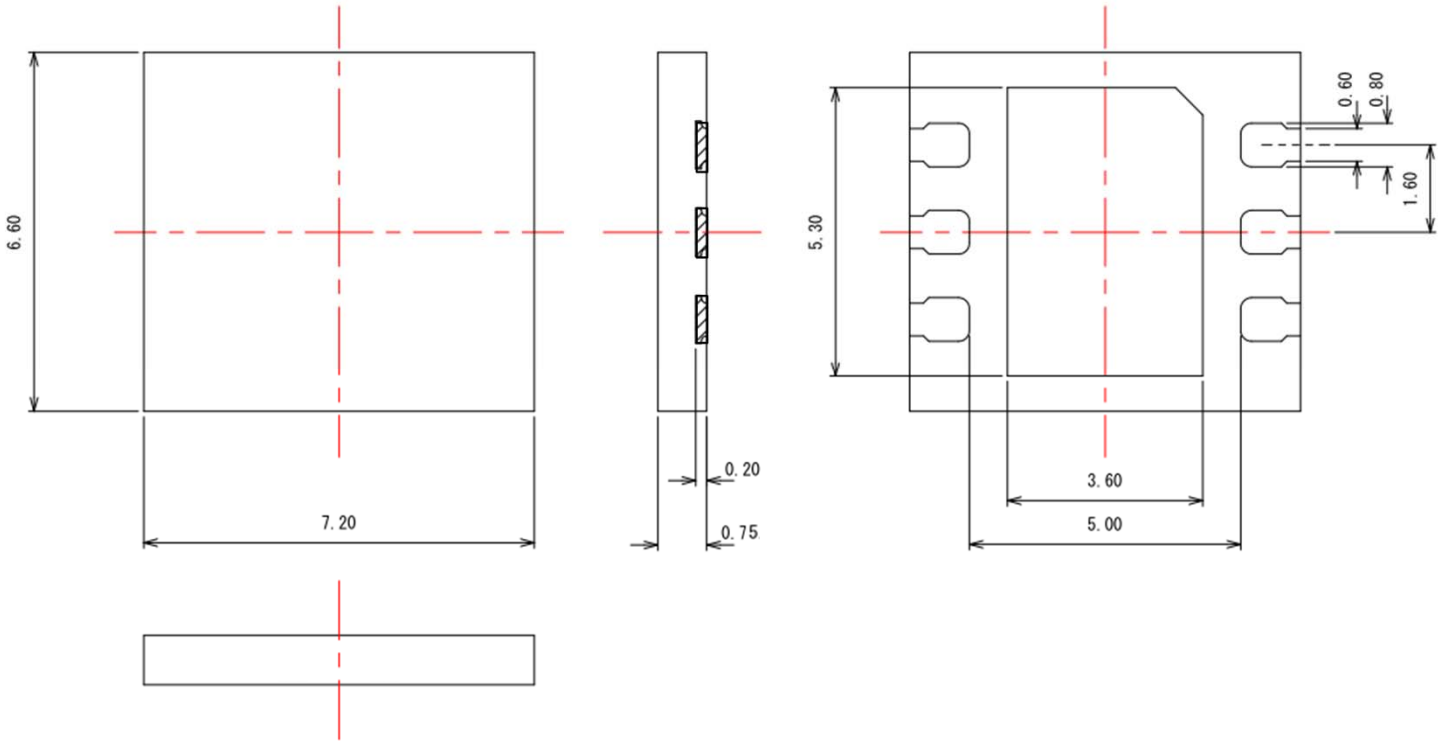
Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Vp	Pinch-Off Voltage	VDS = 50V, ID = 1.2mA	- 2.3	- 1.8	- 1.3	V
Psat*1	Saturated Output Power*1	VDS = 50V, ID(DC) = 30mA f=3.5GHz, Single Path, @ Psat	36.5	38.0	-	dBm
ηdmax*1	Drain Efficiency*1		-	60	-	%
Gp	Linear Power Gain	VDS = 50V, ID(DC) = 30mA f=3.5GHz, Single Path, @ Po = 30.0dBm	17	18	-	dB
ηd	Drain Efficiency		20	25	-	%
ACLR*2	Adjacent Channel Leakage Ratio*2		-	-40	-	dBc
VSWR*1	Load Mismatch Tolerance*1	VSWR=10:1, All Phases,	No Device Degradation			
Rth	Thermal Resistance	ΔVf Method, Single Path	-	-	11.7	°C/W
HBM	Human Body Model	JEDEC JESD22-A114	TBD			
CDM	Charge Device Model	JEDEC JESD22-C101	TBD			
MSL	Moisture Sensitivity Level	JEDEC J-STD-020	3			

*1 : 10%-duty RF Pulse

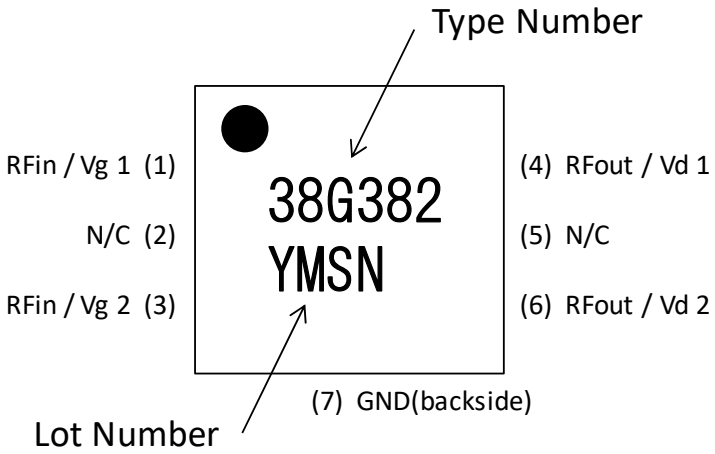
*2 : Signal condition (W-CDMA, Test Model 1 64DPCH, PAPR=7.5dB @0.01% CCDF)

PRODUCT DIMENSIONS

1. Package Drawing [unit : mm]



2. Pin Configuration and Marking



Pin Description

Pin No.	Pin Name	Function
1	RFin / Vg 1	Path 1 RF Input & Gate Voltage
2	N / C	No Function
3	RFin / Vg 2	Path 2 RF Input & Gate Voltage
4	RFout / Vd 2	Path 2 RF Output & Drain Voltage
5	N / C	No Function
6	RFout / Vd 1	Path 1 RF Output & Drain Voltage
7	GND	Ground

Symbol	Content	Description
Y	Year	This single figure shows the year when the assembly of the lot is started. The period of the year is from April to March. (e.g.) 5 -- The lot was assembled in Apr./2015 to Mar./2016
M	Month	This single figure shows the month when the assembly of the lot is started. Apr.=1, May=2, ….. Nov.=8, Dec.=9, Jan.=X, Feb.=Y, Mar.=Z
SN	Serial Number	This combination of double alphabets (expect I,O) shows the order when the assembly of the lot is started in the month.

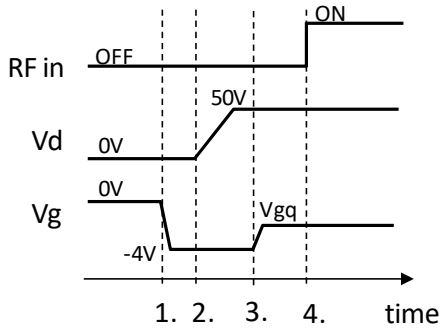
Static Electric Safety Cautions

Compared to silicon products, GaN - and GaAs - based FETs are the products that are more sensitive to the electro-static discharge (ESD). Applying ESD may lead the product to fail. Please handle the product with careful taking ESD counter measures, such as the wrist band, grounding table/floor , ionizer, etc.

Bias On/Off Sequence

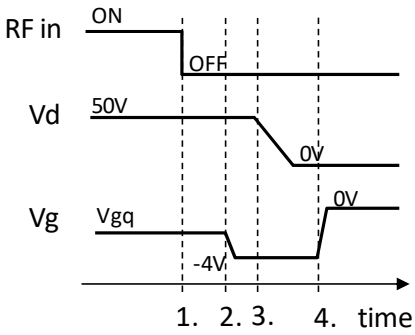
A. Bias sequence for turning on the device

1. Set gate voltage (Vg) to -4V (typically pinch-off voltage).
2. Set drain voltage (Vd) from 0V to 50V.
3. Set gate voltage (Vg) to adjust a drain current (Idq).
4. RF on



B. Bias sequence for turning off the device

1. RF off
2. Set gate voltage to -4V for drain current (Idq) of 0A.
3. Set drain voltage to 0V.
4. Set gate voltage to 0V.



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