

LNA_024_004

24-GHz Low-Noise Amplifier in Silicon Germanium Technology

Data Sheet

| | | | | |
|------------------|--------------------------------|--|--|------------------|
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| Version: 2.1 | Product number: LNA_024_004 | Package: QFN16, 3 × 3 mm ² | Marking: LNA004 YYWW | Page: 1 of 13 |

Version Control

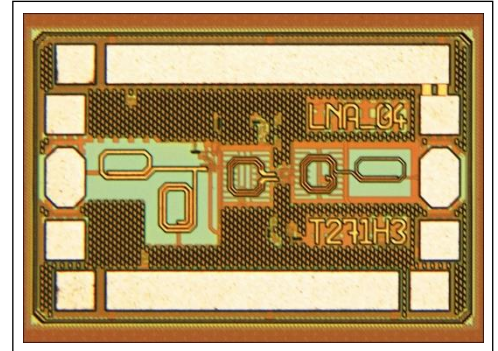
| Version | Changed section | Description of change | Reason for change |
|---------|---|--|--|
| 1.2 | Product name | Changed from LNA_024_05 to LNA_024_004 | New procedure for product nomenclature |
| 2.0 | Specification | Spec data revised, typos fixed, new package drawing. | Routinely revision |
| 2.1 | Application Pin Description IO Stages | Figure 6, Application Circuit: Switch at Vctrl input modified. Description of pins PWR, Vctrl refer to Figure 9. Figure 9, Equivalent I/O Circuits: Diode in series with pull-down resistor shown. | Clarification |

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1 Features

- Low-noise amplifier (LNA) for 24-GHz ISM band
- Single supply voltage of 3.3 V
- Low power consumption of 18 mW
- Fully ESD protected device
- Gain control input
- Power-down mode
- Fast on / off switching for pulsed operation
- QFN16 leadless plastic package 3 mm × 3 mm
- Pb-free, RoHS compliant package
- IC is available as bare die as well



1.1 Overview

The low-noise amplifier LNA_024_004 is a two stage amplifier operating in two gain modes (high gain and low gain) with a power-down feature. The first stage employs a cascode configuration with inductive load and inductive emitter degeneration for stability reasons. The input matching network of the LNA consists of shunt inductor and series capacitor. The input shunt inductor provides ESD protection. In order to provide compact design and galvanic isolation between amplifier stages, transformers were used for interstage coupling and output matching. The second stage is a common-base structure with two gain states. This stage is loaded with a transformer providing appropriate output impedance. The gain mode is defined by an external digital signal at the Vctrl input. The LNA can be powered down via the PWR pin.

1.2 Applications

The main use of the LNA is in wireless communication systems and in radar systems for the ISM band at 24 GHz and for UWB systems up to 29 GHz.

2 Block Diagram

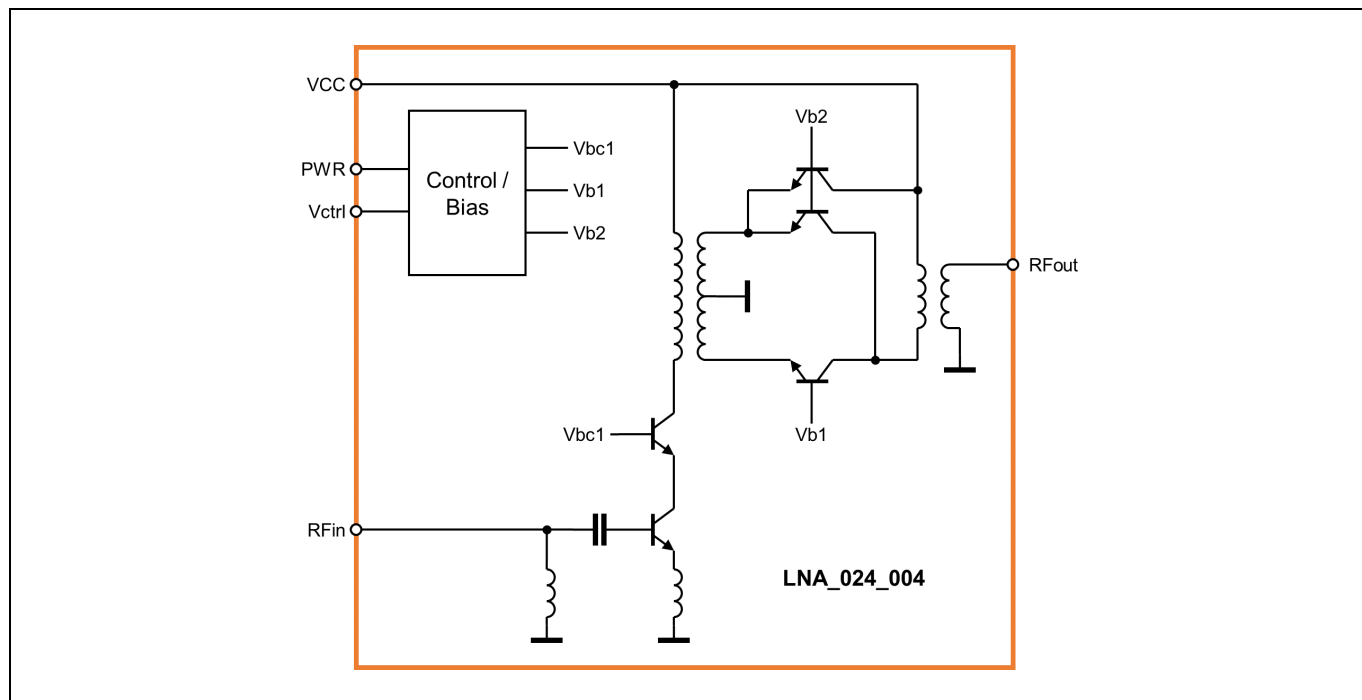


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

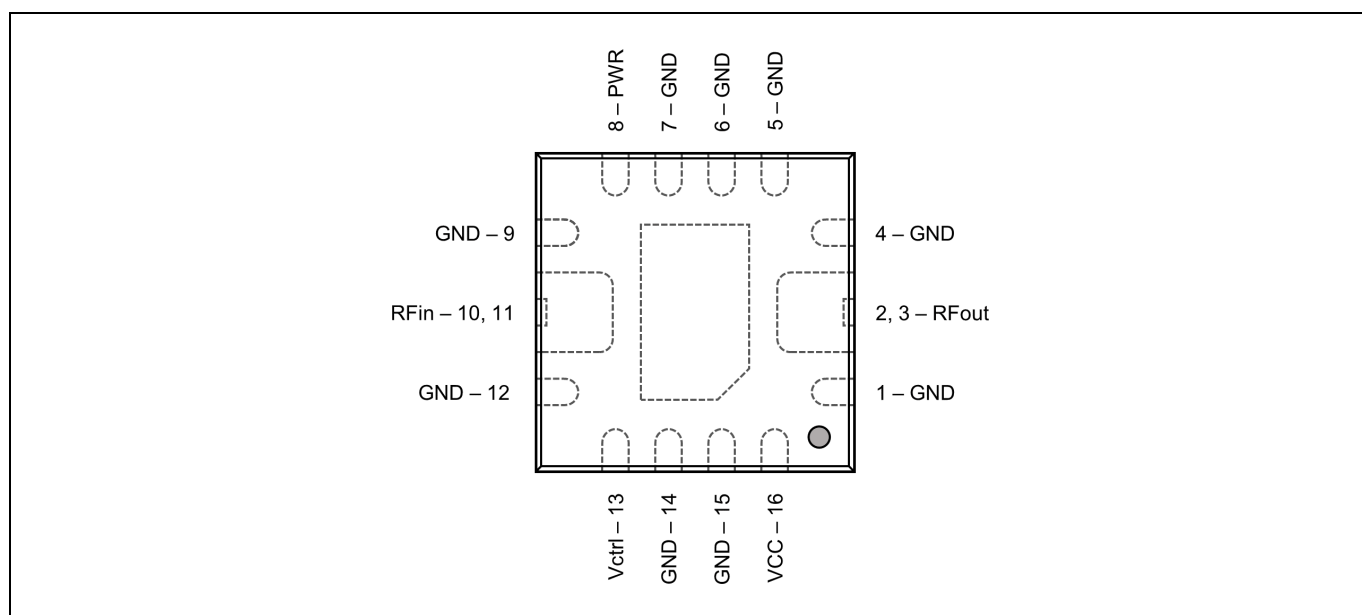


Figure 2 Pin Assignment (QFN16, 3 mm × 3 mm, Top View)

3.2 Pin Description

Table 1 Pin Description

| Pin | | Description |
|------|-------|---|
| No. | Name | |
| 1 | GND | Ground |
| 2 | RFout | RF output, 50 Ω. Pin 2 and 3 have to be shorted on board close to the QFN package. (See recommended land pattern in Figure 4.) |
| 3 | RFout | |
| 4 | GND | Ground |
| 5 | GND | |
| 6 | GND | |
| 7 | GND | |
| 8 | PWR | Power-down input: high – power-down, low – operate. CMOS logic input with pull-down resistor as shown in Figure 9, Equivalent I/O Circuits. |
| 9 | GND | Ground |
| 10 | RFin | RF input, 50 Ω. Pin 10 and 11 have to be shorted on board close to the QFN package. (See recommended land pattern in Figure 4.) |
| 11 | RFin | |
| 12 | GND | Ground |
| 13 | Vctrl | LNA gain control input: high – high gain, low – low gain. CMOS logic input with pull-down resistor as shown in Figure 9, Equivalent I/O Circuits. |
| 14 | GND | Ground |
| 15 | GND | |
| 16 | VCC | Supply voltage, 3.3 V |
| (17) | GND | Exposed die attach pad of the QFN package, must be soldered to ground. |

4 Specification

4.1 Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Table 2 Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Unit | Condition / Remark |
|------------------------------|------------------------------|------|-----------------------|------|---|
| Supply voltage | V _{CC} | | 3.6 | V | to GND |
| DC voltage at RF pins | V _{D_{CRF}} | 0 | 2 | mV | IC provides low ohmic circuit to GND for pin RFout and RFin |
| Junction temperature | T _J | | 150 | °C | |
| Storage temperature range | T _{STG} | -65 | 150 | °C | |
| DC voltage at control inputs | V _{CTL} | -0.3 | V _{CC} + 0.3 | V | Pin Vctrl and PWR |
| Input power into pin RFin | P _{IN} | | 0 | dBm | |
| ESD robustness | V _{ESD} | | 500 | V | Class 1A ¹⁾ |

Note 1 According to ESDA / JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing, Human Body Model Component Level, ANSI / ESDA / JEDEC JS-001-2011

4.2 Operating Range

Table 3 Operating Range

| Parameter | Symbol | Min | Max | Unit | Condition / Remark |
|------------------------------|-----------|------|----------|------|--------------------|
| Ambient temperature | T_A | -40 | 85 | °C | |
| Supply voltage | V_{CC} | 3.13 | 3.47 | V | (3.3V ± 5%) |
| DC voltage at control inputs | V_{CTL} | 0 | V_{CC} | V | Pin Vctrl and PWR |

Note: Do not drive input signals without power supplied to the device.

4.3 Thermal Resistance

Table 4 Thermal Resistance

| Parameter | Symbol | Min | Typ | Max | Unit | Condition / Remark |
|---|------------|-----|-----|-----|------|--------------------|
| Thermal resistance from junction to soldering point | R_{thJS} | | | 50 | K/W | |

4.4 Electrical Characteristics

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise noted. Typical values measured at $T_A = 25^\circ\text{C}$ and $V_{CC} = 3.3\text{ V}$.

Table 5 Electrical Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Condition / Remark |
|---------------------------------|---------------------|---------------------|------|---------------------|------|---|
| DC Parameters | | | | | | |
| Supply current consumption | I_{CC} | 5 | 5.6 | 6.5 | mA | $V(Vctrl) = V(PWR) = 0$ |
| Logic input voltage, low level | V_{IN_L} | 0 | | $0.3 \times V_{CC}$ | V | |
| Logic input voltage, high level | V_{IN_H} | $0.7 \times V_{CC}$ | | V_{CC} | V | |
| Logic input current, low level | I_{IN_L} | -1 | | 1 | μA | $V(Vctrl) = V(PWR) = 0$ |
| Logic input current, high level | I_{IN_H} | 30 | 64 | 150 | μA | $V(Vctrl) = V(PWR) = 3.3\text{ V}$ |
| RF Parameters | | | | | | |
| Frequency range | f_{3dB} | 21.5 | | 28.7 | GHz | |
| Output impedance | Z_{TXout} | | 50 | | Ω | |
| Number of LNA gain settings | N_G | | 2 | | | controlled by input Vctrl |
| LNA gain, high gain | S_{21H} | 13.5 | 15 | 17 | dB | at 24.15 GHz, $V(Vctrl) = 3.3\text{ V}$ |
| LNA gain, low gain | S_{21L} | 6.5 | 8 | 10 | dB | at 24.15 GHz, $V(Vctrl) = 0$ |
| Noise figure, high gain | NF_H | | 3.2 | | dB | $V(Vctrl) = 3.3\text{ V}$, simulated |
| Noise figure, low gain | NF_L | | 5 | | dB | $V(Vctrl) = 0$, simulated |
| Input return loss | $ S_{11} $ | 0.3 | 0.4 | 0.5 | | at 24.15 GHz |
| | $\text{Ph}(S_{11})$ | 157 | 177 | 197 | deg | |
| Output return loss | $ S_{22} $ | 0.4 | 0.5 | 0.6 | | |
| | $\text{ph}(S_{22})$ | -155 | -140 | -125 | deg | |
| Input Compression Point | CP_I | -10 | | -6.5 | dBm | |

5 Packaging

5.1 Outline Dimensions

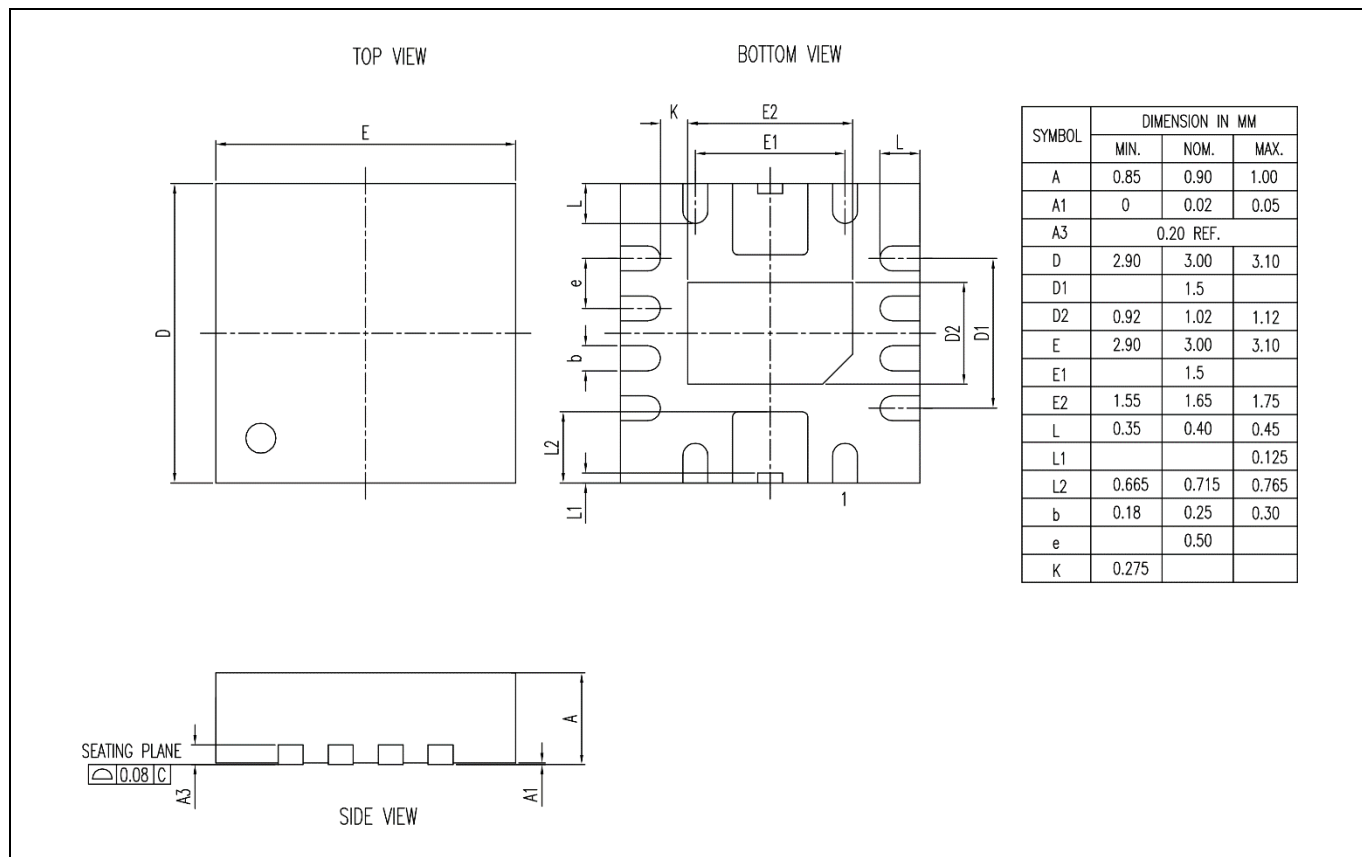


Figure 3 Outline Dimensions of QFN16, 3 mm x 3 mm, 0.5 mm Pitch

5.2 Package Footprint

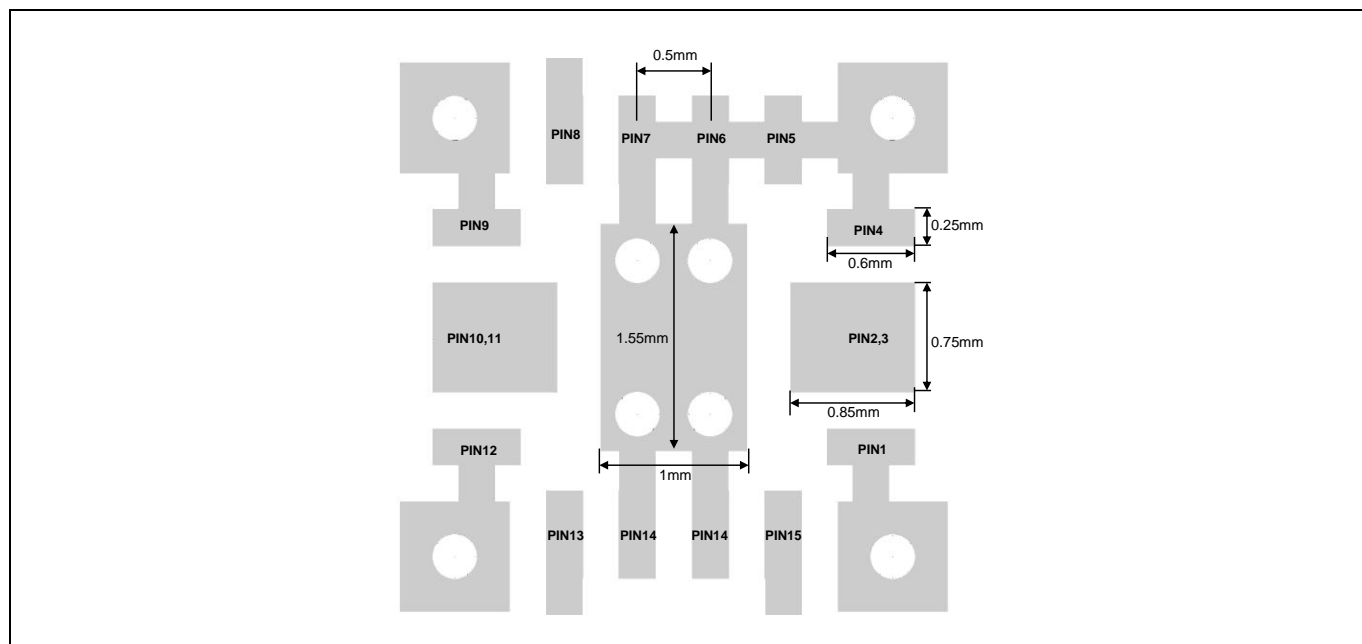


Figure 4 Recommended Land Pattern

5.3 Package Code

Top-Side Marking LNA004
 YYWW

5.4 Qualification Test

Table 6 Reliability and Environmental Test

| Qualification Test | JEDEC Standard | Condition | Pass / Fail |
|--------------------|----------------|-------------------------------------|-------------|
| MSL3 | J-STD-020E | Reflow simulation 3 times at 260 °C | pass |

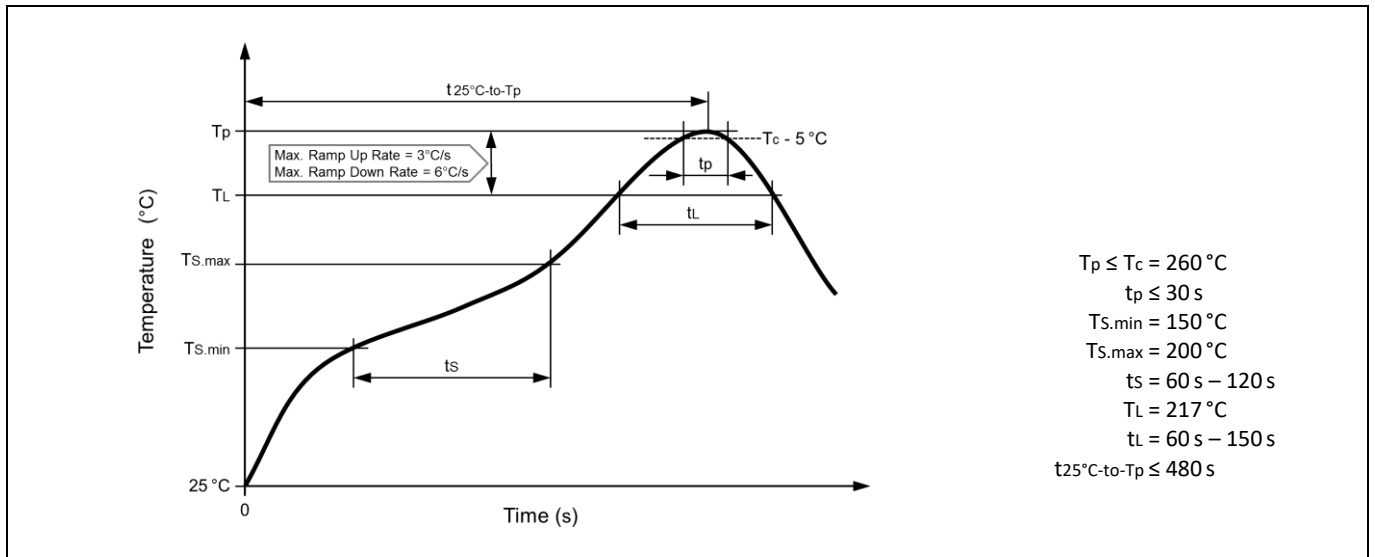


Figure 5 Reflow Profile for Pb-Free Assembly according to JEDEC Standard J-STD-020E

6 Application

6.1 Application Circuit Schematic

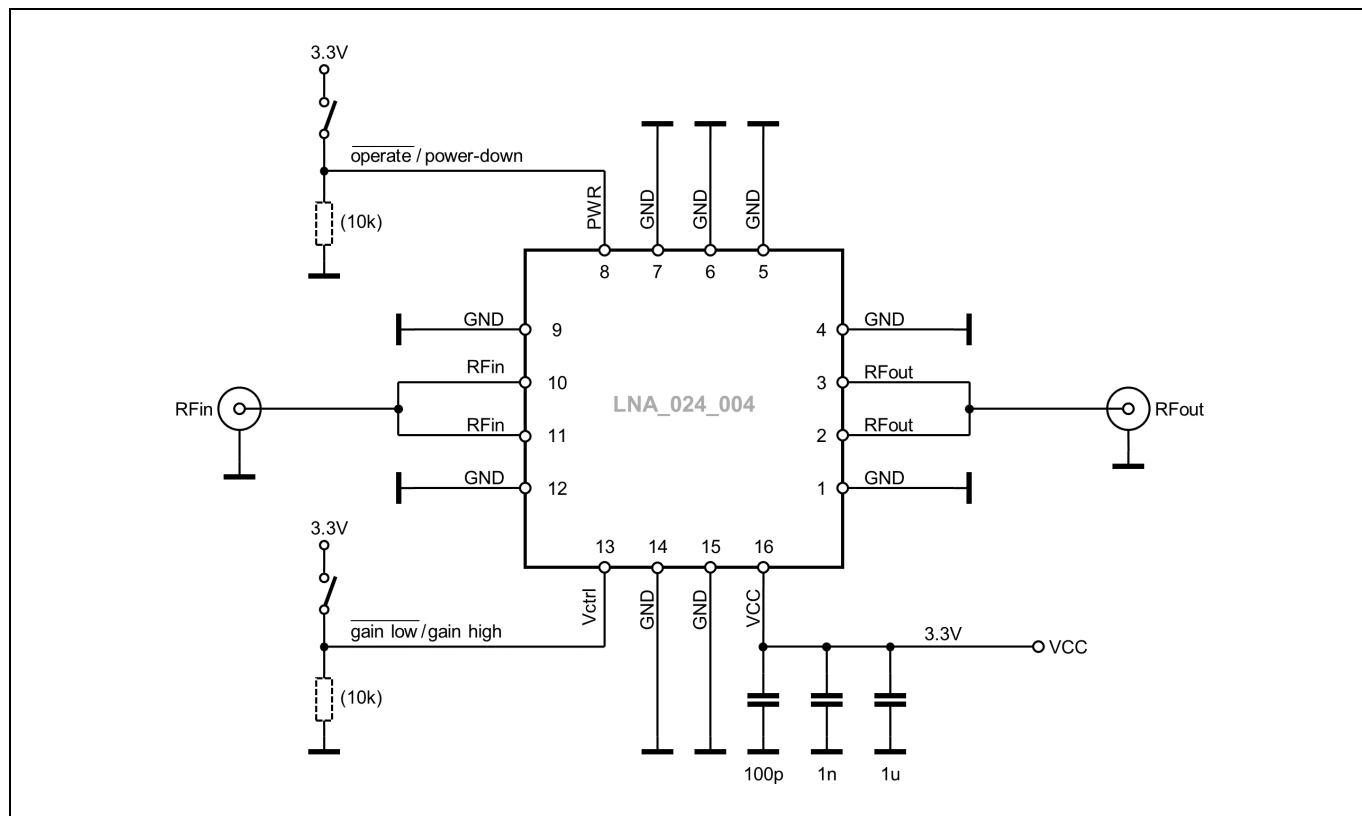


Figure 6 Application Circuit

6.2 Evaluation Board

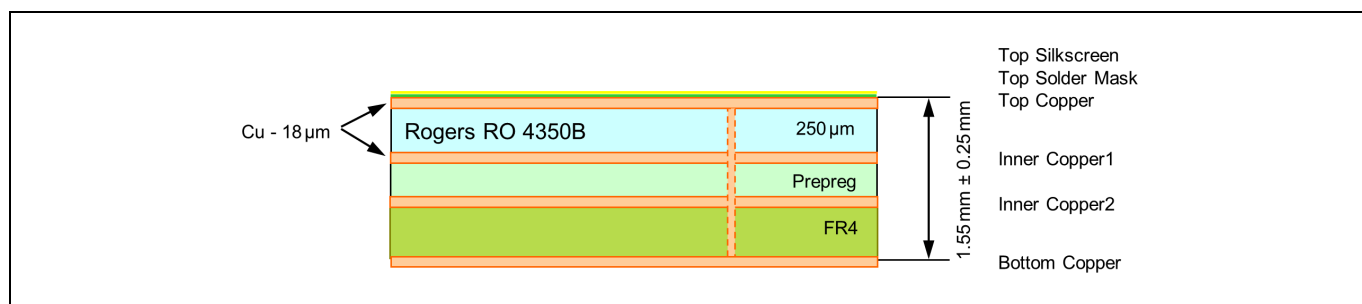


Figure 7 Evaluation Board Stack-up

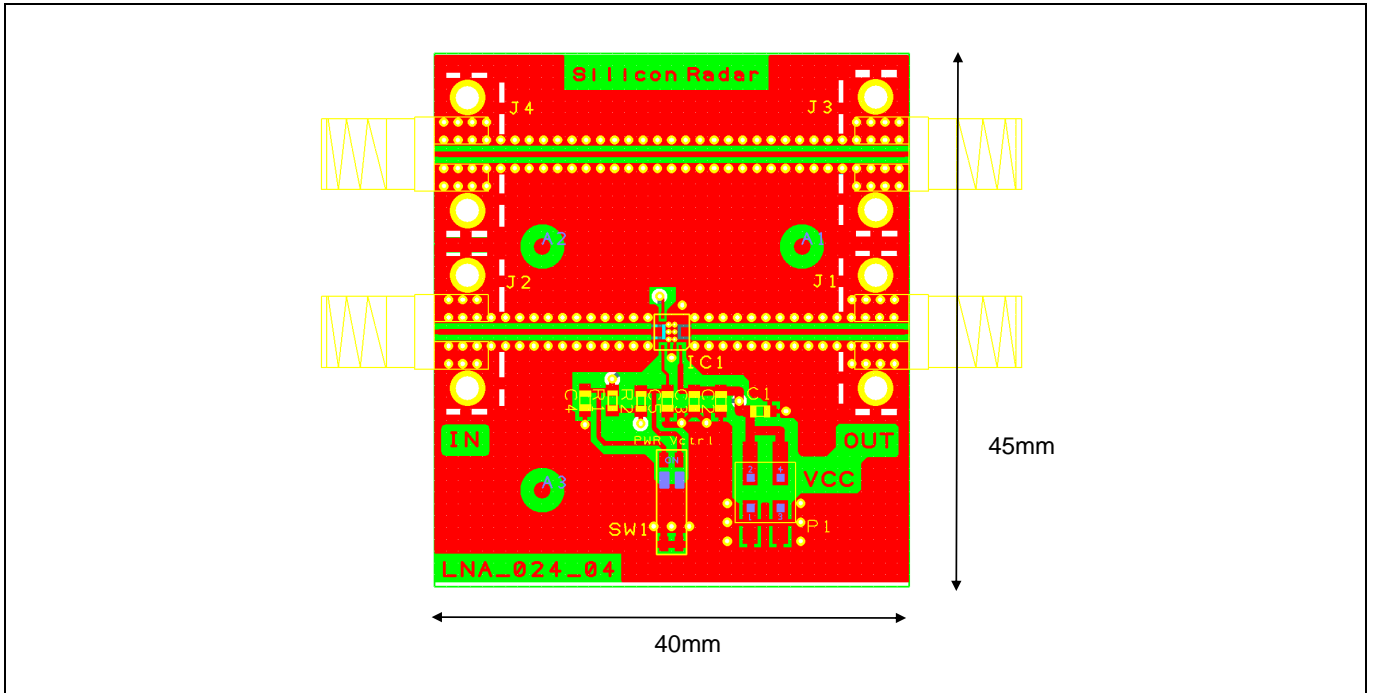


Figure 8 Evaluation Board Layout Including Via Holes (Top View)

6.3 Input / Output Stages

The following figures show the simplified circuits of the input and output stages. It is important that the voltage applied to the input pins should never exceed V_{CC} by more than 0.3 V. Otherwise, the supply current may be sourced through the upper ESD protection diode connected at the pin.

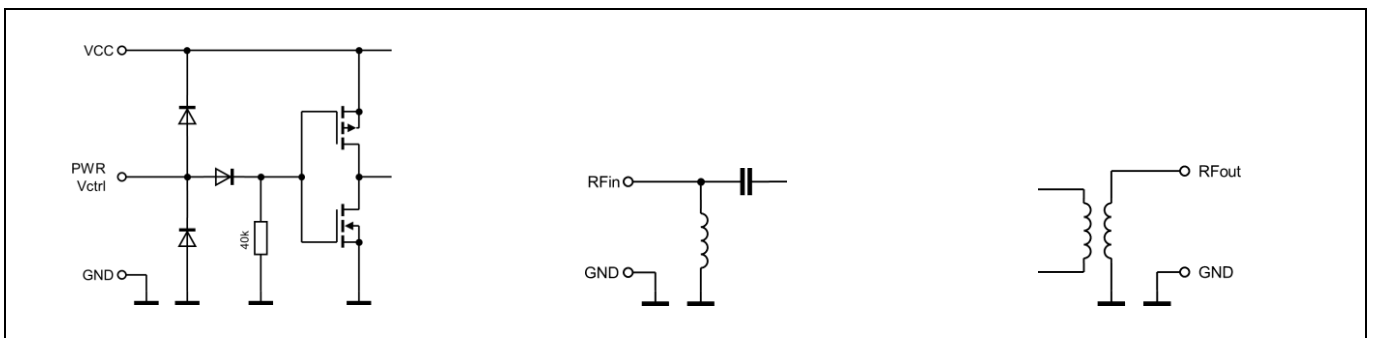


Figure 9 Equivalent I/O Circuits

7 Measurement Results

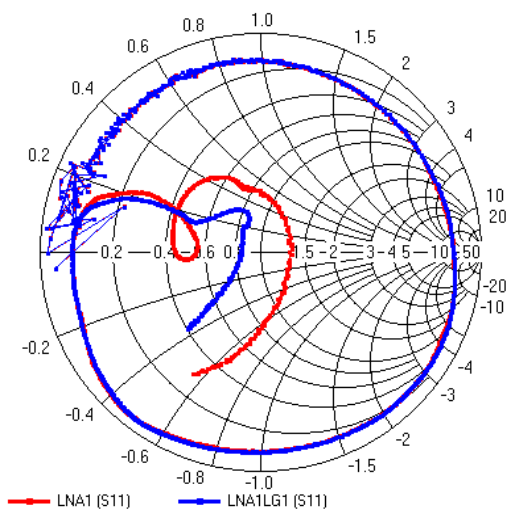


Figure 10 Input Reflection Coefficient, low and high gain

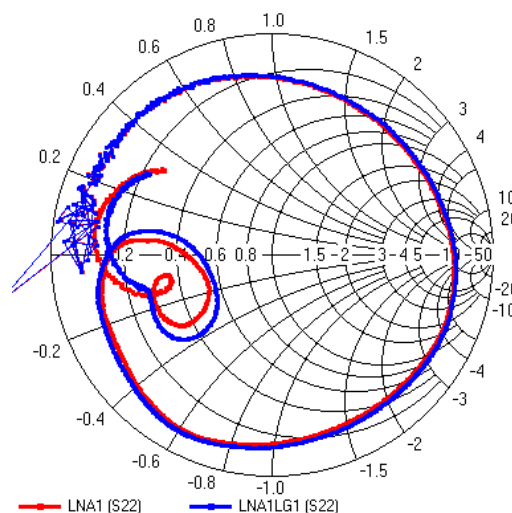


Figure 11 Output Reflection Coefficient, low and high gain

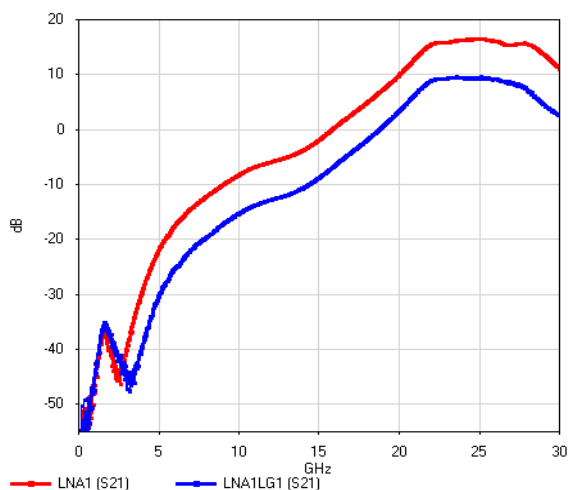


Figure 12 Gain, low and high gain

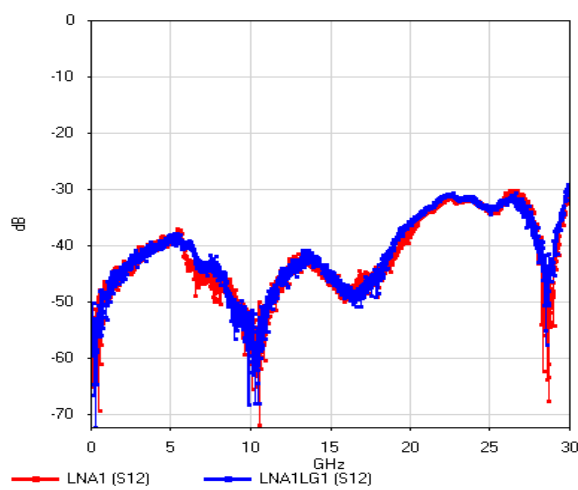


Figure 13 Isolation, low and high gain

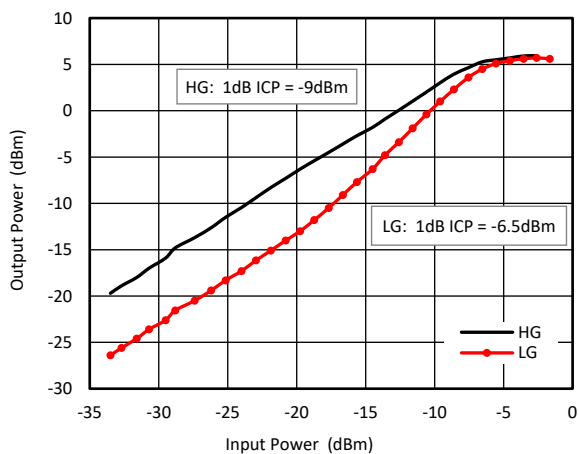


Figure 14 Linearity, low and high gain

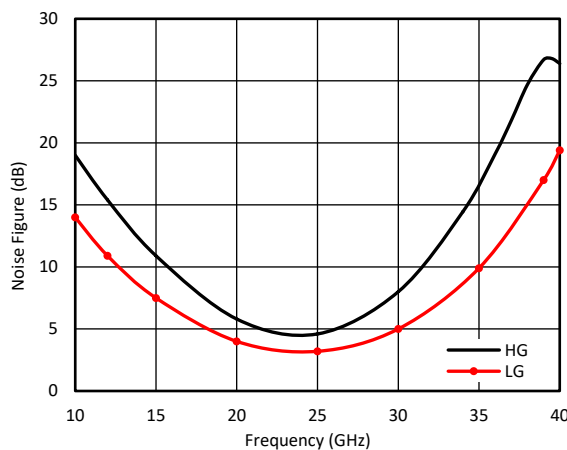


Figure 15 Simulated Noise Figure, low and high gain

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